WHAT IS CLAIMED IS:

1. A method for testing a semiconductor integrated circuit, wherein, when a signal for measuring a delay is applied to a measurement path on which a delay test is conducted, a signal having a transition being in phase or in opposite phase with said signal for measuring a delay applied to said measurement path is applied to a path that influences crosstalk to said measurement path, thereby measuring a propagation delay time of said signal that propagates through said measurement path under the influence of crosstalk.

2. The method according to claim 1, further comprising the steps of:

supplying said signal for measuring a delay to said measurement path after a signal level of said path that influences crosstalk to said measurement path is set to a fixed value, thereby, measuring the propagation delay time of said signal for measuring a delay that propagates through said measurement path; and

performing a quantitative evaluation on the influence of crosstalk, on the basis of a difference between the propagation delay time measured after the signal level of said path that influences crosstalk to said measurement path is set to the fixed value and the propagation delay time of said signal for measuring a delay, measured with the signal applied to said path that influences crosstalk to said measurement path.

3. A method for testing a semiconductor integrated circuit in an AC test using a scan path, the method comprising the steps of:

receiving from a scan-in terminal of a scan path register a pattern for supplying a signal for measuring a delay to a measurement path on

which a delay test is conducted and a pattern for supplying a signal having a transition being in phase or in opposite phase with said signal for measuring a delay to a path that influences crosstalk to said measurement path;

supplying said signal for measuring a delay to said measurement path and supplying the signal to the path that influences crosstalk to said measurement path from said scan path register; and

reading out a value of the scan path register that samples said signal at an end terminal of said measurement path, from a scan-out terminal to compare the value of said scan path register with an expected value, thereby measuring a delay time in said measurement path.

4. A method for testing a semiconductor integrated circuit having a scan path, the method comprising the steps of:

supplying a signal for measuring a delay to a measurement path of a combinational circuit from a flip-flop associated with said measurement path, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting the scan path, and also supplying to a path (termed an aggressor path) that influences crosstalk to said measurement path a signal having a transition being in phase or in opposite phase with said signal supplied to said measurement path from a flip-flop associated with the aggressor path; and

comparing a value of a flip-flop that samples the signal of an end terminal of said measurement path with an expected value, thereby measuring a delay time in said measurement path.

5. A method for testing a semiconductor integrated circuit having a scan path, the method comprising the steps of:

supplying a signal for measuring a delay to a measurement path in a combinational circuit from a flip-flop associated with said measurement path, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting the scan path, and also supplying to a path that influences crosstalk to a clock signal path a signal having a transition being in phase or in opposite phase with said clock signal, a clock to one or plural flip-flop associated with said measurement path being supplied through said clock signal path; and

comparing a value of the flip-flop that samples the signal at an end terminal of said measurement path with an expected value, thereby measuring a delay time in said measurement path.

6. The method according to claim 4, further comprising the steps of:

supplying a signal for setting said path that influences crosstalk to said measurement path to a fixed value from the flip-flop associated with said path so as to measure a delay time in said measurement path; and

evaluating an effect of crosstalk on the basis of a difference between the delay time in said measurement path measured after the signal for setting said path to the fixed value is applied and the delay time in said measurement path measured with the signal applied to said path that influences crosstalk to said measurement path.

7. A method for generating patterns for testing a semiconductor

integrated circuit having a scan path circuit by a computer, the method comprising the steps of:

generating information on a path(termed an aggressor path) that influences crosstalk to a measurement path of a combinational circuit for measuring a delay, on the basis of layout information on said semiconductor integrated circuit, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path; and

generating a pattern for causing a flip-flop associated with said measurement path to output a signal supplied to said measurement path for measuring a delay, and generating a pattern for causing a flip-flop associated with said aggressor path to output a signal supplied to said aggressor path for checking on influence of crosstalk to said measurement path.

8. A method for generating patterns for testing a semiconductor integrated circuit having a scan path circuit by a computer, the method comprising the steps of:

(a) extracting one or plural adjacent paths on the basis of layout information on said semiconductor integrated circuit to extract information on a path that influences crosstalk;

(b) generating measurement path information on a measurement path in a combinational circuit for measuring a delay, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path, said measurement path information including a combination of nodes

constituting said measurement path and transition information of a signal at respective nodes, and generating aggressor path information comprising node information on a path(termed an aggressor path) that influences crosstalk to said measurement path, by referring to said extracted information on crosstalk; and

(c) generating a pattern for outputting a signal that should be set for allowing a signal for measuring a delay supplied to said measurement path to propagate through said measurement path, said pattern being outputted from an associated flip-flop of a register on an input side of said measurement path, and generating a pattern for outputting a signal that should be set so as to be supplied to said aggressor path for influencing crosstalk to said measurement path for propagation through said aggressor path from an associated flip-flop of a register on an input side of said aggressor path, on the basis of circuit information on said semiconductor integrated circuit, said measurement path information, and said aggressor path information.

9. An apparatus for generating patterns for testing a semiconductor integrated circuit having a scan path circuit, the apparatus comprising:

means for generating information on a path (termed an aggressor path) that influences crosstalk to a measurement path of a combinational circuit for measuring a delay, on the basis of layout information on said semiconductor integrated circuit, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path; and

means for generating a pattern for causing a flip-flop associated

with said measurement path to output a signal supplied to said measurement path for measuring a delay, and generating a pattern for causing a flip-flop associated with said aggressor path to output a signal supplied to said aggressor path for checking on influence of crosstalk to said measurement path.

10. An apparatus for generating patterns for testing a semiconductor integrated circuit having a scan pass circuit, the apparatus comprising:

means for extracting adjacent wiring paths on the basis of layout information on said semiconductor integrated circuit to extract information on a path that influences crosstalk;

means for generating measurement path information on a measurement path of a combinational circuit for measuring a delay, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path, said measurement path information comprising a combination of nodes constituting said measurement path and transition information of a signal at the nodes, and generating aggressor path information comprising node information on the path that influences crosstalk to said measurement path, by referring to said extracted information on crosstalk; and

means for generating a pattern for outputting a signal that should be set for allowing a signal for measuring the delay to propagate through said measurement path, said pattern being outputted from an associated flip-flop of a register on an input side of said measurement path, and generating a pattern for outputting a signal that should be set so as to be

supplied to said aggressor path for influencing crosstalk to said measurement path for propagation through said aggressor path from an associated flip-flop of a register on an input side of said aggressor path, on the basis of circuit information on said semiconductor integrated circuit, said measurement path information, and said aggressor path information.

11. A method for testing a semiconductor integrated circuit having a scan path circuit as a device under test with an LSI tester, the method comprising:

(a) a first step for setting said semiconductor integrated circuit to a scan mode to serially supply from a scan-in terminal on said semiconductor integrated circuit initialization patterns,

said initialization patterns including:

a pattern for initializing a flip-flop with an output terminal thereof connected to an input terminal of a measurement path in a combinational circuit for measuring a delay and a path (termed an aggressor path) that influences crosstalk to said measurement path, respectively, the combinational circuit having an input terminal thereof connected to an output terminal of a register comprised of one or plural flip-flops constituting a scan path and an output terminal thereof connected to an input terminal of a register comprised of one or plural flip-flops constituting said scan path;

a pattern for setting one or plural flip-flops that should be set so as to influence statuses of the input terminals of said measurement path and said aggressor path to undergo transitions from the initial states to

predetermined states, the one or plural flip-flops being connected through a combinational circuit to data input terminals of said flip-flops; and

a pattern for setting one or plural flip-flops that should be set so as to cause signals to propagate through said measurement path and said aggressor path to predetermined states;

(b) a second step for setting said semiconductor integrated circuit from the scan mode to a normal mode to cause the flip-flop that outputs the signal to the input terminal of said measurement path to latch a signal applied to a data input end thereof on a first clock, thereby causing the output signal thereof to be changed from the initial state and also to cause the flip-flop that outputs the signal to the input end of said aggressor path to latch a signal applied to a data input terminal thereof on the first clock, thereby causing the output signal thereof to be changed from the initial state, and then causing the flip-flop that receives at a data input terminal thereof the signal at an output end of said measurement path to receive the outputted signal at the data input terminal thereof on a second clock;

(c) a third step for setting said semiconductor integrated circuit to the scan mode again to read out values of the flip-flops that constitutes the scan path from a scan-out terminal arranged on said semiconductor integrated circuit, and then comparing the value of the flip-flop that receives the outputted signal outputted from the output end of said measurement path at the data terminal thereof with an expected value; and

(d) decreasing a clock period by a predetermined period of time if a result of said comparison is a pass, and increasing the clock period by a predetermined period of time if the result of said comparison is a fail, executing the first, second, and third steps, and then determining the clock period at a transition time when the result of said comparison has changed from the pass to the fail, or from the fail to the pass, to be the delay time in said measurement path under the influence of crosstalk.

12. A method for testing a semiconductor integrated circuit having a scan path circuit as a device under test with an LSI tester as a testing device, the method comprising:

(a) a first step for setting said semiconductor integrated circuit to a scan mode to serially supply from a scan-in terminal on said semiconductor integrated circuit initialization patterns,

said initialization patterns including:

a pattern for initializing a flip-flop with an output terminal thereof connected to an input terminal of a measurement path of a combinational circuit for measuring a delay, said combinational circuit having an input terminal thereof connected to an output terminal of a register comprising one or plural flip-flops constituting a scan path and an output terminal thereof connected to an input terminal of a register comprising one or plural flip-flops constituting said scan path;

a pattern for initializing a flip-flop connected to a path that influences crosstalk to a clock signal path for supplying a clock to a flip-flop connected to said measurement path, said path that influences crosstalk being hereinafter referred to as an aggressor path;

a pattern for setting one or plural flip-flops that should be set so as to cause a status of the input terminal of said measurement path to be changed from the initial state, to predetermined states, the one or plural flip-flops being connected to respective data terminals of said flip-flops through a combinational circuit;

a pattern for setting one or plural flip-flops that should be set so as to cause an input terminal of said aggressor path to be changed from the initial state to a state in phase or in opposite phase with the clock, to predetermined states; and

patterns for setting one or plural flip-flops that should be set so as to cause signals to propagate through said measurement path and said aggressor path to predetermined states;

(b) a second step for setting said semiconductor integrated circuit from the scan mode to a normal mode to cause the flip-flop that outputs the signal to the input end of said measurement path to latch a signal applied to a data input terminal thereof on a first clock, thereby causing the output signal to be changed from the initial state and also to cause the flip-flop that outputs the signal to the input terminal of said aggressor path to latch a signal applied to a data input terminal thereof on the first clock, thereby causing the output signal to be changed from the initial state, and then causing the flip-flop that receives from a data input terminal thereof the signal at an output end of said measurement path to receive the output signal at the data input terminal thereof on a second clock;

(c) a third step for setting said semiconductor integrated circuit to

the scan mode again to read out values of the flip-flops that constitutes the scan path from a scan-out terminal on said semiconductor integrated circuit, and then comparing the value of the flip-flop that receives the outputted signal outputted from the output terminal of said measurement path at the data terminal thereof with an expected value; and

(d) a fourth step for decreasing a clock period by a predetermined period of time if a result of said comparison is a pass, and increasing the clock period by a predetermined period of time if the result of said comparison is a fail, executing the first, second, and third steps, and then determining the clock period at a transition time when the result of said comparison has changed from the pass to the fail, or from the fail to the pass, to be the delay time in said measurement path with an effect of crosstalk.

13. The method according to claim 11, further comprising the steps of:

supplying a signal for setting said path that influences crosstalk to said measurement path to a fixed value from the flip-flop associated with the path so as to measure a delay time in said measurement path; and

evaluating the influence of crosstalk on the basis of a difference between the delay time in said measurement path measured after the signal for setting said path to the fixed value is supplied and the delay time in said measurement path measured with the signal supplied to said path that influences crosstalk to said measurement path.

14. A computer program product for causing a computer to execute processes for generating patterns for testing a semiconductor circuit

having a scan path circuit, the program product comprising the processes of:

(a) generating information on a path (termed an aggressor path) that influences crosstalk to a measurement path of a combinational circuit for measuring a delay, on the basis of layout information on said semiconductor integrated circuit, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path; and

(b) generating a pattern for causing a flip-flop associated with said measurement path to output a signal supplied to said measurement path for measuring a delay, and generating a pattern for causing a flip-flop associated with said aggressor path to output a signal supplied to said aggressor path for checking on influence of crosstalk to said measurement path.

15. A computer program product for causing a computer to execute processes for generating patterns for testing a semiconductor circuit having a scan path circuit, the program product comprising the processes of:

(a) extracting adjacent one or plural paths on the basis of layout information on said semiconductor integrated circuit to extract information on a path that influences crosstalk;

(b) generating measurement path information on a measurement path of a combinational circuit for measuring a delay, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path, said

measurement path information comprising a combination of nodes constituting said measurement path and transition information of a signal at the nodes, and generating path information comprising node information on the path(termed an aggressor path) that influences crosstalk to said measurement path, by referring to said extracted information on crosstalk; and

(c) generating a pattern for outputting a signal that should be set for allowing a signal for measuring a delay to propagate through said measurement path, said pattern being outputted from an associated flip-flop of a register on an input side of said measurement path, and generating a pattern for outputting a signal that should be set so as to be supplied to said aggressor path for influencing crosstalk to said measurement path and for propagation through said aggressor path from an associated flip-flop of a register on an input side of said aggressor path, on the basis of circuit information on said semiconductor integrated circuit, said measurement path information, and said aggressor path information.

16. A computer program product for causing a computer to execute processes for generating patterns for testing a semiconductor circuit having a scan path circuit, the program product comprising the processes of:

(a) extracting adjacent one or plural paths on the basis of layout information on said semiconductor integrated circuit to extract information on a path that influences crosstalk;

(b) generating measurement path information on a measurement

path of a combinational circuit for measuring a delay, the combinational circuit being disposed between a plurality of registers, each of which comprises one or plural flip-flops constituting a scan path, said measurement path information comprising a combination of nodes constituting said measurement path and transition information of a signal at the nodes, and generating path information comprising node information on a path (termed an aggressor path) that influences crosstalk to a clock signal path for supplying a clock to a flip-flop associated with said measurement path, if said path exists, said path that influences crosstalk, by referring to said extracted information on crosstalk; and

(c) automatically generating a pattern for outputting the signal that should be set for allowing a signal for measuring the delay to propagate through said measurement path from an associated flip-flop of a register on an input side of said measurement path, and generating a pattern for outputting a signal that should be set so as to be supplied to said aggressor path for influencing crosstalk to said measurement path for propagation through said aggressor path from an associated flip-flop of a register on an input side of said aggressor path, on the basis of circuit information on said semiconductor integrated circuit, said measurement path information and said clock signal path information, and said aggressor path information.

17. The method according to claim 5, further comprising the steps of:

supplying a signal for setting said path that influences crosstalk to said measurement path to a fixed value from the flip-flop associated

with said path so as to measure the delay in said measurement path; and

evaluating an effect of crosstalk on the basis of a difference between the delay in said measurement path measured after the signal for setting said path to the fixed value is applied and the delay in said measurement path measured with the signal applied to said path that influences crosstalk to said measurement path.

18. The method according to claim 12, further comprising the steps of:

supplying a signal for setting said path that influences crosstalk to said measurement path to a fixed value from the flip-flop associated with the path so as to measure the delay in said measurement path; and

evaluating the influence of crosstalk on the basis of a difference between the delay in said measurement path measured after the signal for setting said path to the fixed value is supplied and the delay in said measurement path measured with the signal supplied to said path that influences crosstalk to said measurement path.